ABSTRACT

A processor includes dependency checking logic and a register stack having a top register and other registers. The processor is configured to override the dependency logic such that operations related to the register stack are operable to be executed in parallel. Parallel execution may include substantially simultaneously switching the contents of the top register of the register stack with contents of another register of the register stack and vice versa, such that an error does not occur. The processor is further configured to execute an algorithm that replaces the contents of the top register, the other register, or both the top and other registers with a defined architectural response if an exception occurs when the content of both registers are switched.